REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on February 10, 2006, and the references cited therewith.

Applicant has amended claims 1, 10, 15, 17-19, 22, 23 and 34 are amended. Claims 17, 18, 22, 23 and 34 have been amended merely to address matters of form. Claims 1, 10, 15 and 19 have been amended to further clarify the subject matter which Applicant regards as his invention. Applicant has not canceled or added any claims. Accordingly, claims 1-37 remain pending in this application.

Claim Rejections – 35 U.S.C. § 102

In the Office Action, the Examiner rejected claims 1-2, 4, 10-11, 24-28, 32-35 and 37 under 35 US.C. § 102(b) as being anticipated by "Phase and Frequency Detectors for Clock Synchronization in High-speed Optical Transmission Systems.", Sari et al., European Transactions on Telecommunications and Related Technologies, vol. 5, no. 5, September – October 1994, pp. 101-107 (hereafter "Sari"). Applicant respectfully traverses this rejection.

Claim 1, as amended, recites:

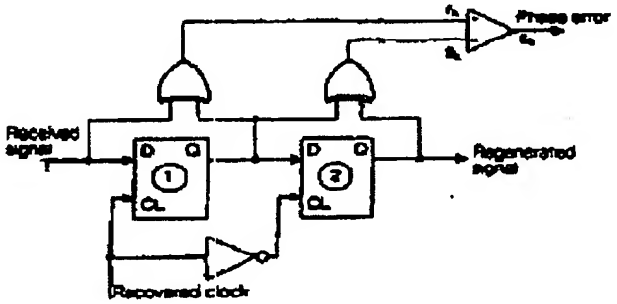
> A binary phase detector comprising:
> a first flip flop comprising:
> a data input coupled to a first signal having a first frequency, and
> a clock input coupled to a second signal having a second frequency and a phase relationship with the first signal, wherein the first frequency is a multiple of the second frequency; and
> a second flip flop comprising:
> a data input coupled to an output of the first flip flop, and
> a clock input coupled to the second signal at substantially the phase relationship with the first signal.

As is well settled, in order to establish anticipation under § 102, each an every element of a rejected claim must be present in a single prior art reference. Applicant respectfully submits that Sari does not include each and every element of claim 1 and, therefore, does not anticipate claim 1.

Claim 1 is directed to a binary phase detector that includes a first flip flop and a second flip flop. The first flip flop has a data input coupled to a first signal and a clock input coupled to a second signal, where the second signal has a phase relationship with the first signal. The

second flip flop of the binary phase detector of claim 1 includes a data input coupled with an output of the first flip flop and a clock input coupled to the second signal at substantially the phase relationship with the first signal. Sari does not describe or disclose (explicitly or inherently) such a binary phase detector and, therefore, cannot anticipate claim 1.

Sari discloses a phase detector in FIG. 5 on which the Examiner relied in rejecting claim 1. For the Examiner's convenience, Applicant presents FIG. 5 of Sari below.



In comparison with claim 1, the phase detector of Sari includes a first flip flop "1" that has a data input coupled with a "Received signal" and a clock input coupled with a "Recovered clock" signal. The phase detector of Sari's FIG. 5 also includes a second flip flop "2" that has a data input coupled with an output of the first flip flop. Sari's second flip flop includes a clock input that is coupled to an inverted version of the "Recovered clock" signal. Because the clock input of the second flip flop is coupled with an inverted version of the "Recovered clock" signal, the phase relationship of the signal received at the clock input of the second flip flop will be 180 degrees out of phase with the signal received at the clock input of the first flip flop. Accordingly, Sari discloses a first flip flop with a clock input that is coupled with a second signal and a second flip flop with a clock input that is coupled with a signal (e.g., third signal or inverted version of the second signal) that is 180 degrees out of phase with the second signal.

Such an approach does not disclose or describe the binary phase detector of claim 1, which includes (i) a first flip flop with a clock input that is coupled with a second signal, where the second signal has a phase relationship with a first signal (e.g., a signal provided to a data input of the first flip flop) and (ii) a second flip flop with a clock input that is coupled with the second signal at substantially the phase relationship with the first signal. The signals provided to the clock inputs of the first and second flip flops of Sari's phase detector are 180 degrees out of

phase with respect to each other and, accordingly, have substantially different phase relationships with the "Received signal" in Sari's FIG. 5.

Based on the foregoing, Sari does not anticipate claim 1 as Sari fails to disclose or describe each and every element of claim 1. Therefore, Applicant respectfully requests that the Examiner withdraw the rejection of claim 1.

Without addressing the Examiner's remarks with respect to claims 2, 4 and 24-28, which are not conceded, Applicant notes that these claims depend from claim 1 and include all of its limitations and the limitations of any intervening claims. Therefore, Sari does not anticipate claims 2, 4 and 24-28 by virtue of their dependency on claim 1. Applicant respectfully requests that the Examiner withdraw the rejection of claims 2, 4 and 24-28.

Applicant has amended claim 10 in similar fashion as claim 1. Therefore, Sari does not anticipate claim 10 for the same reasons discussed above with respect to claim 1. Applicant respectfully requests that the Examiner withdraw the rejection of claims 10.

Without addressing the Examiner's remarks with respect to claims 11, 32-35 and 37, Applicant notes that these claims depend from claim 10 and include all of its limitations and the limitations of any intervening claims. Therefore, Sari does not anticipate claims 11, 32-35 and 37 by virtue of their dependency on claim 10. Applicant respectfully requests that the Examiner withdraw the rejection of claims 11, 32-35 and 37.

Claim Rejections – 35 U.S.C. § 103

In the Office Action, the Examiner also rejected claims 12, 15 and 19-20 under 35 U.S.C. § 103(a) as being obvious over U.S. Patent 6,388,485 to Kim in view of Sari. Applicant respectfully addresses this rejection.

The Examiner cites Kim as disclosing a delay locked loop and asserts that the phase detector of Sari could be used in the circuit of Kim. Kim does not, however, make up for deficiencies of Sari described above. For instance, implementing the phase detector of Sari in the circuit of Kim, conceding for purposes of argument that such a combination is proper, would produce a delay locked loop with a phase detector including two flip flops, where the first flop includes a clock input coupled with a signal (i.e., the "Recovered clock" signal) and the second

flip flop includes a clock input coupled with an inverted version of the signal (i.e., an inverted version of the "Recovered clock" signal).

As is well settled, in order to establish a *prima facie* case of obviousness based on multiple references, when combined, the combination must include each an every element of the rejected claims. The combination of Kim and Sari fails to disclose each and every element of the rejected claims as the proposed combination does not disclose or even suggest a delay locked loop (or phase locked loop) including a phase detector that includes a first flip flop with a clock input that is coupled with a second signal, where the second signal has a phase relationship with a first signal (e.g., a signal provided to a data input of the first flip flop) and a second flip flop with a clock input that is coupled with the second signal at substantially the phase relationship with the first signal, as was described above with respect to claims 1 and 10. Accordingly, claims 1 and 10 are not obvious over Kim in view of Sari.

Claim 12 depends from claim 10 and includes all of its limitations. Therefore, based on the foregoing, claim 12, by virtue of its dependency on claim 10, is not obvious over Kim in view of Sari. Applicant respectfully requests that the Examiner withdraw the rejection of claim 12.

Applicant has amended independent claims 15 and 19 in substantially similar fashion as claims 1 and 10, as discussed above. Therefore, claims 15 and 19 are not obvious over Kim in view of Sari for substantially the same reasons set forth above. Applicant respectfully requests that the Examiner withdraw the rejection of claims 15 and 19.

Without addressing the Examiner's remarks with respect to claim 20, Applicant notes that this claim depends from claim 19 and includes all of its limitations. Therefore, claim 20 is not obvious over Kim in view of Sari by virtue of its dependency on claim 19. Applicant respectfully requests that the Examiner withdraw the rejection of claim 20.

Allowable Subject Matter

The Examiner indicated the allowance of claims 3, 7-9, 17-18, 22-23 and 30-31.

The Examiner objected to claims 5-6, 13-14, 16, 21, 29 and 36 as being dependent upon a rejected base claim, but indicated these claims to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant thanks the Examiner for these indications of allowance and allowability. However, because Applicant believe, in view of the foregoing amendments and remarks, that all pending claims are allowable, Applicant has elected not to amend 5-6, 13-14, 16, 21, 29 and 36 in independent form.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect earnestly requests and notification to that effect. Applicant invites the Examiner to telephone Applicant's attorney (703-286-5303) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 50-3521.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this paper is being transmitted by facsimile to the U.S. Patent and Trademark Office on the date shown below.

Paul Churilla

July 10, 2006
Date of Transmission